In the claims:

Please amend claims 1, 2, 8, 9, 13, 14, 15, and 16 as follows:

1. (TWICE AMENDED) An apparatus [for converting signals of a first preselected voltage level to a second preselected voltage level], comprising:

a transistor having an enable terminal, an input terminal, and an output terminal, said input terminal **for** receiving [said] signals [of the] **that vary between** first **and second** preselected voltage [level] **levels**, and said output terminal **for** delivering [said] signals [of the second] **that vary between the first** preselected voltage level **and a third preselected voltage level**;

a capacitor coupled across said input and output terminals of said transistor; and

a resistive element having a first end portion coupled to the enable terminal of said transistor and a second end portion [coupled] **for coupling** to a voltage supply **to bias the transistor continuously on, the resistive element cooperating with a parasitic capacitor defined by said transistor to temporarily increase the voltage applied to the enable terminal during a transition from the first to the second preselected voltage level at the input terminal**.

2. (AMENDED) An apparatus, as set forth in claim 1, including a buffer circuit having an input terminal coupled to receive said signals **that vary between the first and third** [of the second] preselected voltage **levels**.

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8. (TWICE AMENDED) An apparatus for converting **digital** signals **that vary between 0 volts and** [of] a first preselected voltage level **to digital signals that vary between 0 volts and** [to] a second preselected voltage level, comprising:

a pass gate transistor having a gate, source, and drain, said drain **for** receiving said signals **that vary between 0 volts and** [of] the first preselected voltage level, said source **for** delivering said signals **that vary between 0 volts and** [of] the second preselected voltage level, said gate coupled to a voltage supply having a third preselected voltage level;

a capacitor coupled across said source and drain of said pass gate transistor; and

a pump coupled to the gate of said pass gate transistor, said pump being configured to ~~temporarily~~ increase the voltage level applied to said gate **during a transition from 0 volts to the first preselected voltage level**.

9. (TWICE AMENDED) An apparatus, as set forth in claim 8, wherein said pump includes a resistive element coupled between the gate of said pass gate transistor and said voltage supply, and a capacitor coupled to the gate of said pass gate transistor [and receiving] **to receive said digital signals that vary between 0 volts and the first preselected voltage level** [said input signal].

13. (TWICE AMENDED) An apparatus for converting an input signal **that varies between** [of a] first **and second** preselected voltage **levels** [level] to **an output signal that varies between the first preselected voltage level and a third** [a second] preselected voltage level, comprising:

a pass gate transistor having a gate, source, and drain, said drain **for** receiving said **input** signals [of the first preselected voltage level], said source **for** delivering said **output** signals [of the second preselected voltage level], said gate being coupled to a voltage supply having a [third] **fourth** preselected voltage level;

a capacitor coupled across said source and drain of said pass gate transistor; and

means for ~~temporarily~~ increasing the voltage level applied to said gate **during a transition of the input signal from the first to the second preselected voltage level**.

14. (AMENDED) An apparatus, as set forth in claim 13, wherein said means includes means for increasing the voltage level applied to said gate for a preselected period of time [during a transition in said input signal from a logically low voltage level to a logically high voltage level].

15. (AMENDED) A method for converting an input signal **that varies from 0 volts to** [of] a first preselected voltage level to **an output signal that varies from 0 volts to** a second preselected voltage level, comprising:

charging a gate of a pass gate transistor to a third preselected voltage level to enable the pass gate transistor to pass at least a portion of the [voltage level of the] input signal to an output node;

charging the gate of the pass gate transistor to a fourth preselected voltage level for a preselected period of time, said fourth preselected voltage level being greater than said third preselected level; and

passing at least a portion of any AC component in said input signal to said output node.

16. (AMENDED) A method, as set forth in claim 15, wherein charging the gate of the pass gate transistor to a fourth preselected voltage level includes charging the gate of the pass gate transistor to a fourth preselected voltage level for a preselected period of time during a transition in said input signal from **0 volts** [a logically low voltage level] to **the first preselected** [a logically high] voltage level.

Please add new claims 17-20 as follows:

17. (NEW) A buffer circuit, comprising:

a pass gate transistor having a gate, source, and drain, said drain coupled to receive a first digital signal that varies between first and second voltage levels;

a first voltage supply coupled to the gate of said pass gate transistor to bias the transistor continuously on;

a capacitor coupled across the source and drain of said pass gate transistor;

an inverter having an input terminal and an output terminal, said input terminal coupled to the source of said pass gate transistor to receive a second digital signal that varies between the first voltage level and a third voltage level; and

a pull-up transistor having a source coupled to a second voltage supply, a drain coupled to the source of said pass gate transistor, and a gate coupled to the output terminal of said inverter.

18. (NEW) The buffer circuit of claim 17, further comprising a resistive element coupled between said first voltage supply and the gate of said pass gate transistor, the resistive element cooperating with a parasitic capacitor defined by the drain and gate of said pass gate transistor to ~~temporarily~~ increase the applied voltage to the gate of said pass gate transistor.

19. (NEW) The buffer circuit of claim 18, wherein the resistive element comprises a resistor.

20. (NEW) The buffer circuit of claim 18, wherein the resistive element comprises a PMOS-type transistor having a gate coupled to ground, a drain coupled to the gate of the pass gate transistor, and a source coupled to the first voltage supply.